


Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2457	SERIAL NO. 10/735,355	
<div style="display: flex; align-items: center;"> <div> <p>LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)</p> </div> </div>				APPLICANT: Zhongze Wang		
				FILING DATE December 12, 2003	GROUP 2811	
U.S. PATENT DOCUMENTS						
*Examiner's Initials	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
QU	AA	6,245,636	6/12/2001	Maszara		
QU	AB	2002/0048844	4/25/2002	Sakaguchi		
CK	AC	2002/0034844	3/21/2002	Hsu et al.		
	AD					
	AE					
	AF					
	AG					
	AH					
	AI					
	AJ					
	AK					
	AL					
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)						
AM						
AN						
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AP						
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EXAMINER		DATE CONSIDERED				
Quinn		M. Kennedy August 26, 2005				
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Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. M122-2457	SERIAL NO. 10/735,355
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U.S. PATENT DOCUMENTS							
Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
JM	AA	6,048,411	4/2000	Henley et al.			
JM	AB	6,071,783	6/2000	Liang et al.			
JM	AC	6,091,076	7/2000	Deleonibus			
JM	AD	6,245,729	2/2002	Maszara			
JM	AE	6,346,729	2/2002	Liang et al.			
JM	AF	6,358,791	3/2002	Hsu et al.			
JM	AG	6,403,485	6/2002	Quek et al.			
JM	AH	6,649,959	11/2003	Hsu et al.			
JM	AI	6,664,146	12/2003	Yu			
JM	AJ	2002/004884	4/2002	Sakaguchi			
JM	AK	2002/0034844	3/2002	Yusukawa			
JM	AL	10/924,776		Ford			08/25/2004

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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)			
JM	AM		Bashir et al., <i>Characterization of sidewall defects in selective epitaxial growth of silicon</i> , 13 J. VAC. SCI. TECHNOL. B, No. 3, pp. 923-927 (May/June 1995).
JM	AN		Bashir et al., <i>Reduction of sidewall defect induced leakage currents by the use of nitrided field oxides in silicon selective epitaxial growth</i> ..., 18 J. Vac. Sci. Technol. B, No. 2, pp. 695-699 (March/April 2000).
JM	AO		Hammad et al., <i>The Pseudo-Two-Dimensional Approach to Model the Drain Section in SOI MOSFETs</i> ,
			48 IEEE TRANSACTIONS ON ELECTRON DEVICES, No. 2, pp. 386-387 (February 2001).
JM	AP		Sivagnaname et al., <i>Stand-by Current in PD-SOI Pseudo-nMOS Circuits</i> , IEEE, pp. 95-96 (2003)
JM	AO		Wang et al., <i>Achieving Low Junction Capacitance on Bulk SI MOSFET Using SDOI Process</i> , Micron Technology, Inc., 12 pages (pre-2004).
EXAMINER		DATE CONSIDERED	
J. M. Kennedy		August 24, 2005	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			